CLAIMS

WHAT IS CLAIMED IS:

1.   A vertical sync phase lock loop (PLL), comprising:

a sync detector adapted to output a phase error;

a vertical sync discrete time oscillator (DTO) block adapted to output a vertical sync DTO based on the phase error; and

an output logic adapted to detect a vertical sync based on the vertical sync DTO.

2.   The vertical sync PLL of claim 1 further comprising a loop filter adapted to receive the phase error.

3.   The vertical sync PLL of claim 2, wherein the loop filter further comprises at least one of a following element from a group consisting of:

a first multiplier;

a first adder;

a second multiplier; and

a decay accumulator.

4.   The vertical sync PLL of claim 3, wherein the first multiplier is adapted to multiply a proportional gain constant to the phase error.

5.   The vertical sync PLL of claim 3 further comprising a first accumulator adapted to produce an output, wherein the phase error is added to the output at the adder.

6.   The vertical sync PLL of claim 5 further comprising a first multiplexer and a binary shift block adapted to receive a result of the adding, wherein the binary shift block is adapted to shift the result a number of bits.

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7. The vertical sync PLL of claim 6, wherein the first multiplexer is adapted to receive the shifted result and an output of the phase error through the decay accumulator.

8. The vertical sync PLL of claim 7, wherein a decision logic of the decay accumulator is presented by:

decay acc = ((abs(prev_vsync_phase_error)>7/4*vsync_phase_error) && ((abs(vsync_phase_error)>>21)>6)).

9. The vertical sync PLL of claim 7, wherein a decay condition is based on detection of a rapid change in the phase error provided it is larger than a minimum value.

10. The vertical sync PLL of claim 7 further comprising a second multiplexer, wherein an output of the first multiplexer is input to the second multiplexer.

11. The vertical sync PLL of claim 10, wherein an output of the second multiplexer is received by the first accumulator.

12. The vertical sync PLL of claim 11 further comprising a third multiplier adapted to multiply the output of the first accumulator by a factor, wherein the result from the multiplication is input to the second multiplexer.

13. The vertical sync PLL of claim 12 further comprising a fourth multiplier adapted to multiply the output of the accumulator by a common mode integral gain constant.

14. The vertical sync PLL of claim 13 further comprising a second adder adapted to add an output from the fourth multiplier, with an output from the first multiplier, and with a nominal decrement value.

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15.   The vertical sync PLL of claim 14 further comprising a third multiplexer adapted to receive an output from the second adder.

16.   The vertical sync PLL of claim 3 further comprising a second accumulator adapted to produce an output based on an output of the second multiplier.

17.   The vertical sync PLL of claim 16 further comprising a fifth multiplier adapted to multiply the output from the second accumulator with a differential mode integral gain constant.

18.   The vertical sync PLL of claim 17 further comprising a sixth multiplier adapted to multiply an output from the fifth multiplier with an output from a fourth multiplexer.

19.   The vertical sync PLL of claim 18 further comprising a third adder adapted to add an output form the sixth multiplexer with a vertical sync DTO decrement value.

20.   The vertical sync PLL of claim 19 wherein the addition produces an input into the third multiplexer.

21.   The vertical sync PLL of claim 20 further comprising a   DTO decrement register adapted to receive an output from the third multiplexer.

22.   The vertical sync PLL of claim 21, wherein the DTO decrement register is adapted to send the vertical sync DTO decrement value.